Reply to Office action of June 2, 2004

AMENDMENTS TO THE SPECIFICATION

Please replace the section entitled "Abstract" by deleting the text on page 16 and replacing the deleted section with the following replacement section showing all changes relative to the previous version of the section:

A semiconductor memory testing implementation suitable for build-in self repair (BISR) memories provides-advantages over conventional memory testing techniques. According to , in one embodiment, a memory testing circuit configuration includes including an output register for receiving digital data. A plurality of shift registers serially output the digital data to be received by the output register. Each one of the plurality of shift registers includes a feedback path for enabling the digital data output by a corresponding one of the plurality of shift registers to be input back into the corresponding shift register in a same sequence as the digital data is output from the corresponding shift register.